UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,875	02/19/2004	Shou-Lung Chen	3313-1116P	1953

2292 7590 01/11/2006

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,875	CHEN ET AL.	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27 and 28* is/are allowed.

6)☒ Claim(s) *9-14 and 17-26* is/are rejected.

7)☒ Claim(s) *15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9, 10, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuo et al. (US 2002/0036338, of record).

Matsuo et al. discloses, as shown in Figures 1A-1C and 12, a stacked package for electronic elements, comprising:

a substrate (BS), having a supporting surface, wherein a plurality of stud bumps (TP) are formed on the supporting surface and contact the supporting surface;

an electronic element (SBB,SBA), having a plurality of vias corresponding to the stud bumps, wherein the vias are respectively aligned with the stud bumps to securely mount the electronic element on the substrate.

Regarding claim 10, Matsuo et al. discloses the material of the stud bumps is a conductive metal (solder).

Regarding claim 12, Matsuo et al. discloses the element is silicon chip, a GaAs chip, an InP chip or an epitaxily-grown chip.

Regarding claim 13, Matsuo et al. discloses the substrate is an organic substrate, a ceramic substrate, a glass substrate, a silicon substrate or a GaAs substrate.

2. Claims 9, 10, 13, 14, 18 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Moden et al. (PN 6,297,548, of record).

Moden et al. discloses, as shown in Figures 1-6, a stacked package for electronic elements, comprising:

a substrate (2), having a supporting surface, wherein a plurality of stud bumps (162) are formed on the supporting surface and contact the supporting surface;

an electronic element (100), having a plurality of vias corresponding to the stud bumps, wherein the vias are respectively aligned with the stud bumps to securely mount the electronic element on the substrate.

Regarding claims 10 and 18, Moden et al. discloses the material of the stud bumps is a conductive metal.

Regarding claims 13 and 21, Moden et al. discloses the substrate is an organic substrate, a ceramic substrate, a glass substrate (FR-4), a silicon substrate or a GaAs substrate.

Regarding claim 14, Moden et al. discloses, as shown in Figures 1-6, a stacked packaged for electronic elements, comprising:

a substrate (2), having a supporting surface, wherein a plurality of stud bumps (162) are formed on the supporting surface and contact the supporting surface;

a plurality of electronic elements (100), each having a plurality of vias corresponding to the stud bumps, wherein the vias of each electronic element are respectively aligned with the stud bumps, each of the stud bumps being allowed to pass through the corresponding vias of the plurality of electronic elements so as to securely mount and stack the electronic elements on the substrate.

3. Claims 9-12, 14, 17-20 and 22-26 and are rejected under 35 U.S.C. 102(e) as being anticipated by Glen et al. (PN 6,577,013).

Glen et al. discloses, as shown in Figures 3-16, a stacked package for electronic elements, comprising:

a substrate (39, not illustrated), having a supporting surface, wherein a plurality of stud bumps (42) are formed on the supporting surface and contact the supporting surface;

an electronic element (16), having a plurality of vias corresponding to the stud bumps, wherein the vias are respectively aligned with the stud bumps to securely mount the electronic element on the substrate.

Regarding claims 10 and 18, Glen et al. discloses the material of the stud bumps is a conductive metal.

Regarding claims 11 and 19, Glen et al. discloses the material of the stud bumps is gold, copper or aluminum.

Regarding claims 12 and 20, Glen et al. discloses the element is a silicon chip, a GaAs chip, an InP chip or an epitaxily-grown chip.

Regarding claim 14, Glen et al. discloses, as shown in Figures 1-6, a stacked packaged for electronic elements, comprising:

a substrate (39, not illustrated), having a supporting surface, wherein a plurality of stud bumps (42) are formed on the supporting surface and contact the supporting surface;

a plurality of electronic elements (16), each having a plurality of vias corresponding to the stud bumps, wherein the vias of each electronic element are respectively aligned with the stud bumps, each of the stud bumps being allowed to pass through the corresponding vias of the plurality of electronic elements so as to securely mount and stack the electronic elements on the substrate.

Regarding claim 17, Glen et al. discloses the package further comprising a spacer (54) between adjacent electronic elements.

Regarding claim 22, Glen et al. discloses each of the stud bumps has a bottom wider than a width of the corresponding via.

Regarding claims 23 and 24, Glen et al. discloses each of the stud bumps protrudes from a top surface of the electronic element.

Regarding claim 25, Glen et al. discloses the plurality of electronic elements are stacked from bottom to top as a stacked structure, and each of the stud bumps has a height larger than a height of the stacked structure.

Regarding claim 26, Glen et al. discloses the plurality of electronic elements are stacked from bottom to top as a stacked structure, and each of the stud bumps protrudes from a top surface of the topmost electronic element of the stacked structure.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al. (US 2002/0036338, of record).

Matsuo et al. discloses all of the claimed limitations except material of the stud bumps. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Matsuo et al. having the materials as that claimed by Applicant, since it has been held to be within the general skill of a worker in the art to select a known

material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moden et al. (PN 6,297,548, of record).

Moden et al. discloses all of the claimed limitations except material of the stud bumps. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Matsuo et al. having the materials as that claimed by Applicant, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

6. Claims 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moden et al. (PN 6,297,548, of record) in view of Matsuo et al. (US 2002/0036338, of record).

Moden et al. discloses the chip is a semiconductor chip or die. Moden et al. does not disclose the chip is a silicon chip, a GaAs chip, an InP chip or an epitaxily-grown chip. However, Matsuo et al. discloses a chip (S) is a silicon chip. Note Figures 1A-1C and 12. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the chip of Moden et al. as a silicon chip, such as taught by Matsuo et al. since silicon is conventionally used as a base to form the device thereon.

7. Claims 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glen et al. (PN 6,577,013) in view of Moden et al. (PN 6,297,548, of record).

Glen et al. discloses the claimed invention including the stacked package as explained in the rejection above. Glen et al. does not disclose the material of the substrate. However, Moden et al. discloses a stacked package comprising a substrate (2) having the material as claimed. Note Figures 1-6 of Moden et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate of Glen et al. having the material as claimed, as taught by Moden et al. since these materials are commonly used as the substrate and they are interchangeable.

Allowable Subject Matter

8. Claims 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 27 and 28 are allowed.

Response to Arguments

10. Applicant's arguments filed 10/28/05 have been fully considered but they are not persuasive.

It is argued, at pages 7-9 of the Remarks, that Matsuo et al. and Moden et al. do not disclose the plurality of stud bumps contact the supporting surface. This argument is not convincing because Matsuo et al. and Moden et al. disclose the plurality of stud bumps electrically contact the

supporting surface. Note that the claimed language does not state whether the plurality of stud bumps in directly contact or in physical contact the supporting surface, therefore, Applicants' claim 9 and 14 do not distinguish over the Matsuo et al. and Moden et al. references.

11. Applicant's arguments with respect to claims 1 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Monday to Thursday 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272 - 1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu

January 4, 2005

Hung Vu

Primary Examiner